Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for connecting an integrated circuit to a substrate, the method comprising

providing a first electrical contact structure on the integrated circuit,

providing a second electrical contact structure on the substrate,

at least one of the first and second electrical contact structures having an elastic elevation thereon,

attaching the integrated circuit to a frame structure, the frame structure including a lateral subregion, the lateral subregion at least partially surrounding the integrated circuit and not in contact with a surface of said substrate when said current path is formed

forming a current path between the first electrical contact structure and the second electrical contact structure, and

attaching the frame structure to the substrate, thereby compressing the elastic elevation; wherein attaching the frame structure includes:

applying heat to bring said frame structure in contact with said substrate, such that upon heating, said subregion expands and touches a surface of said substrate, and upon cooling, said subregion remains attached to the surface of said substrate.

2. (Canceled)

3. (Previously Presented) The method according to claim 2, further comprising selecting

said subregion to include a peripheral annular region.

4. (Previously Presented) The method according to claim 2, further comprising selecting

said subregion to include a region with individual discrete supports. ~~an interrupted support region~~.

5. (Canceled)

6. (Canceled)

7. (Previously Presented) The method according to claim 1, further comprising providing a compression stop region on one of said integrated circuit and said substrate.

8. (Previously Presented) The method according to claim 1, further comprising providing metallization on the elastic elevation.

9. (Previously Presented) The method according to claim 2, further comprising providing,

on said frame structure, a planar base region that protrudes laterally beyond the integrated circuit, and

connecting said subregion to the base region such that a space exists between said subregion and said integrated circuit.

10. (Previously Presented) The method according to claim 1, further comprising forming a unitary frame structure in which the subregion and a base region are integral with each other.

11. (Previously Presented) The method according to claim 2, further comprising

adhesively bonding said subregion to said substrate.

12. (Previously Presented) The method according to claim 2, further comprising soldering said subregion to said substrate.

13. (Previously Presented) The method according to claim 1, further comprising bringing said first electrical contact structure and said second electrical contact structure into mechanical contact, such that

said first electrical contact structure and said second electrical contact structure are displaceable with respect to each other in a common plane.

14. (Previously Presented) The method according to claim 1, further comprising disposing said elastic elevation on said first electrical contact structure.

15. (Previously Presented) The method according to claim 14, wherein ~~providing~~ the second electrical contact structure has a planar terminal region.

16. (Previously Presented) The method according to claim 15, further comprising selecting a material having a thermal expansion coefficient of the planar terminal region to be greater than the thermal expansion coefficient of the elastic elevation.

17. (Currently Amended) A circuit arrangement manufactured according to the method of claim 1, the circuit arrangement comprising

a first electrical contact structure on the integrated circuit,

a corresponding second electrical contact structure on the substrate,

the first electrical contact structure being in electrical communication with the second electrical contact structure,

at least one of the first and second electrical contact structures having an elastic elevation thereon,

a frame structure attached to the integrated circuit and the substrate and being disposed to compress the elastic elevation.

~~thereby compressing the elastic elevation.~~

18. (Previously Presented) A circuit arrangement according to claim 17, wherein said frame structure includes a lateral subregion at least partially surrounding the integrated circuit.

19. (Currently Amended) A circuit arrangement according to claim 18 ~~claim 17~~, wherein

said subregion includes a peripheral annular region.

20. (Currently Amended) A circuit arrangement according to claim 18 ~~claim 17~~, wherein

said subregion includes a region with individual discrete supports. ~~an interrupted support region~~.

21. (Previously Presented) A circuit arrangement according claim 17, further comprising

a compression stop region on said integrated circuit.

22. (Previously Presented) A circuit arrangement according to claim 17, further comprising

a metallization layer on the elastic elevation.

23. (Previously Presented) A circuit arrangement according to claim 17, further comprising a planar base region on said frame structure, wherein

said subregion is connected to a base region protruding laterally beyond the integrated circuit such that a space exists between said integrated circuit and the subregion.

24. (Previously Presented) A circuit arrangement according claim 17, wherein said frame structure is a unitary piece.

25. (Previously Presented) A circuit arrangement according to claim 17, further comprising an adhesive between said substrate and said frame.

26. (Previously Presented) A circuit arrangement according to claim 17 further comprising a solder between said substrate and said frame.

27. (Previously Presented) A circuit arrangement according claim 17, wherein

said first electrical contact structure and said second electrical contact structure are in mechanical contact, and

said first electrical contact structure and said second electrical contact structure are displaceable with respect to each other in a common plane.

28. (Previously Presented) A circuit arrangement according claim 17, wherein said elastic elevation is connected to said first electrical contact structure.

29. (Previously Presented) A circuit arrangement according claim 28, wherein said second electrical contact structure has a planar terminal region.

30. (Previously Presented) A circuit arrangement according to claim 29, wherein

the planar terminal region has a thermal expansion coefficient greater than a thermal expansion coefficient of the elastic elevation.

31. (New) A circuit arrangement comprising

a first electrical contact structure on the integrated circuit,

a corresponding second electrical contact structure on a substrate,

the first electrical contact structure being in electrical communication with the second electrical contact structure,

at least one of the first and second electrical contact structures having an elastic elevation thereon, and

a frame structure attached to the integrated circuit and the substrate and being disposed to compress the elastic elevation, the frame structure including a lateral subregion at least partially surrounding the integrated circuit, the subregion including a region with individual discrete supports.

32. (New) A circuit arrangement comprising

a first electrical contact structure on the integrated circuit,

a corresponding second electrical contact structure on a substrate,

the first electrical contact structure being in electrical communication with the second electrical contact structure,

at least one of the first and second electrical contact structures having an elastic elevation thereon,

a frame structure attached to the integrated circuit and the substrate and being disposed to compress the elastic elevation; and

a compression stop region on said integrated circuit.